REMARKS

Claims 1-12 are pending. The specification has been amended. Substitute drawings are being submitted herewith for Figs. 1, 6, 15 and 19. No new matter is presented.

The drawings were objected to under 37 CFR 1.83(a) because the external power source was not shown. Applicant respectfully submits the element 26 in Fig. 1, for example, is the external power source which generates the voltage Vpp. Although the specification refers to element 26 as an external terminal, this should actually state that it is a power source. As stated in paragraph [0085] of the specification, the voltage Vpp is inputted from an external terminal 26. This means that the external terminal outputs the voltage Vpp and must be an external power source. One of ordinary skill in the art would understand that the external terminal is the same thing as an external power source in this case. The specification has been amended throughout to reflect that the external terminal 26 is actually an external power source. Applicants submit that this amendment does not introduce new matter.

Claims 1-10 were rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. In particular, the Examiner notes that claims 1, 7 and 9 refer to the external power source. Applicants believe that the foregoing amendments and explanation render this rejection moot. Accordingly, it is respectfully requested that this rejection be withdrawn.

Claims 2, 4, 6, 8 and 10 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out an distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

The Examiner asserts that the recitation "voltage boosting circuit provided between the external power source and the resistance element" is unclear and confusing. Fig. 6 shows the second embodiment of the invention and is described in the specification beginning at paragraph [0102]. The voltage boosting circuit 41 boosts the voltage received from the external power source 26. This boosted voltage Hvpp is used instead of the voltage Vpp. Fig. 6 has been modified to clarify that the voltage boosting circuit 41 is between the external power source 26 and the resistor 40.

In light of the foregoing, Applicant requests that this rejection be withdrawn.

Claims 1-6, 8, 10, 11 and 12 were rejected under 35 USC 102(b) a being anticipated by Ninomiya, U.S. Patent 5,617,359. This rejection is respectfully traversed.

Claim 1 recites "a resistance element inserted between the regulator circuit and an external power source" and "voltage level detecting means for instructing start of the erase voltage application to the common source line, detecting that an input voltage from the resistance element to the regulator circuit reaches a prescribed voltage level and instructing termination of the erase voltage application to the common source line."

The Examiner asserts that Ninomiya discloses, in Fig. 9, the claimed resistance element. Ninomiya discloses that the embodiment shown in Fig. 9 includes an erase/verify system 25. Ninomiya teaches a variable reference voltage generator 25a. The variable voltage reference generator is coupled between the source of erasing voltage Vpp and ground, and three series combinations of resistor and fuse element are coupled in parallel between the source or erasing voltage Vpp and an output node OUT (col. 11, lines 23-30). The resistors serve to optimize the reference voltage Vref depending on the characteristics of the memory cells (col. 11, lines 37-39). Thus, the resistors only impact the reference voltage Vref, not the claimed input voltage. From this, it is clear that the claimed resistor and the resistors shown in Fig. 9 of Ninomiya serve different functions and have an effect on completely different voltages. Thus, Ninomiya will not achieve the claimed invention. Accordingly, Ninomiya fails to teach or suggest the features of claim 1.

Claims 2-10 and 12 are allowable at least due to their respective dependencies. Claim 11 is allowable for the same reasons claim 1 is allowable. Applicant requests that this rejection be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

In the event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 204552022200.

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Respectfully submitted,

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